Claims

[c1] 1. A process for forming a contact for a semiconductor device comprising:
forming a first compound semiconductor layer, wherein:
the first compound semiconductor layer includes a first compound semiconductor material and has a first conductivity type;
forming a second compound semiconductor layer, wherein the second compound semiconductor layer includes a second compound semiconductor material and has a second conductivity type; and
the second conductivity type is opposite the first conductivity type;
patterning the second semiconductor layer to define an opening with a wall;
forming an insulating material along the wall; and
forming a third compound semiconductor material at least partially within the opening, wherein:
the third compound semiconductor material has the first conductivity type and a dopant concentration that is higher than a dopant concentration of the first compound semiconductor layer; and
the third compound semiconductor material is electrically connected to the first compound semiconductor layer and is insulated from the second compound semiconductor layer.

[c2] 2. The process of claim 1, wherein the third compound semiconductor material is formed by sputtering.

[c3] 3. The process of claim 1, wherein each of the first, second, and third compound semiconductor materials include at least two Group IVA elements.

[c4] 4. The process of claim 1, wherein each of the first, second, and third compound semiconductor materials include silicon carbide.

[c5] 5. The process of claim 1, further comprising forming a metal layer above and electrically connected to the third compound semiconductor material.

[c6] 6. The process of claim 5, wherein an electrical connection between the third compound semiconductor material and the metal layer is ohmic.

[c7] 7. The process of claim 5, wherein the metal layer comprises aluminum.

[c8] 8. The process of claim 1 further comprising forming a third compound semiconductor layer before forming the first compound semiconductor layer, wherein the third compound semiconductor layer includes a fourth compound semiconductor material and has the second conductivity type.

[c9] 9. A semiconductor device comprising:
a first active layer including a first compound semiconductor material and having a first conductivity type;
a second active layer including a second compound semiconductor material and having a second conductivity type opposite the first conductivity type, wherein the second active layer contacts the first active layer;
a third active layer including a third compound semiconductor material and having the first conductivity type, wherein:
the third active layer contacts the second active layer; and
a combination of the first, second, and third active layers are at least part of a transistor;
an opening extending through the third active layer and contacting the second active layer;
a fourth compound semiconductor material at least partially within the opening, wherein the fourth compound semiconductor material:
has the second conductivity type and a dopant concentration higher than a dopant concentration of the second active layer; and
is electrically connected to the second active layer;
and an insulating layer at least partially within the opening, wherein the insulating layer lies between the third active layer and the fourth compound semiconductor material.

[c10] 10. The device of claim 9, where each of the first, second, third, and fourth compound semiconductor material include at least two Group IVA elements.

[c11] 11. The device of claim 9, where the first, second, third, and fourth compound semiconductor material comprise silicon carbide.

[c12] 12. The device of claim 9, further comprising electrical contacts to the third

active layer and the fourth compound semiconductor material.

[c13] 13. The device of claim 12, wherein the electrical contacts are ohmic.

[c14] 14. The device of claim 9, wherein surfaces of the insulating layer and metal contacts furthest from the substrate lie in substantially a same plane.

[c15] 15. The device of claim 9, wherein the second active layer has a thickness in a range of approximately 0.1-2 microns thick.